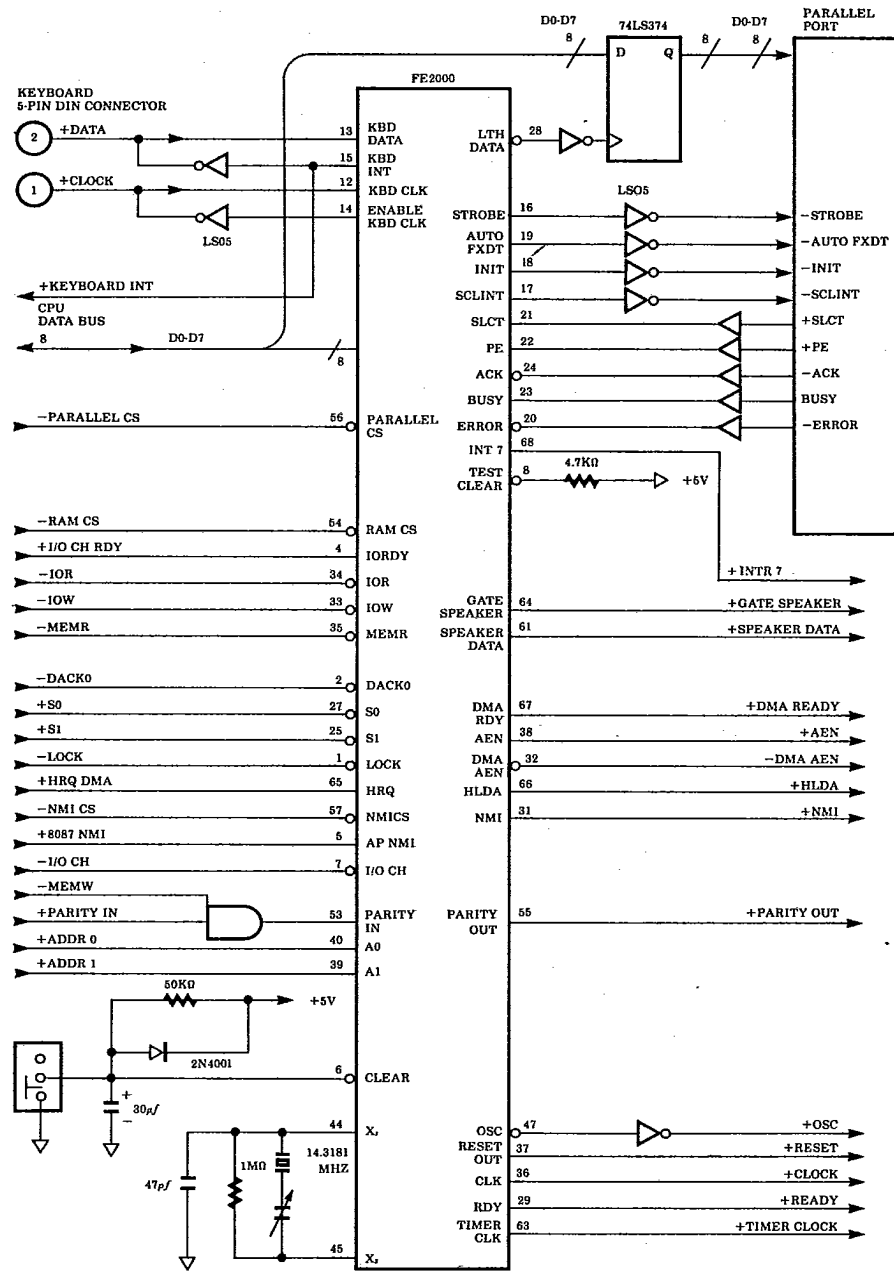


FE2000 APPLICATION

The Faraday CPU Controller (FE2000) is a single chip with various control logic designed to complement the Processor 8088 and to build on an IBM® compatible single board computer. The chip is packaged in a 68 pin J-type leaded surface mount and uses CMOS technology. The chip carrier socket for this plastic chip carrier is available from Burndy (Part #QILE6BP-408).



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B
6/84/5M

The FE2000 is a CPU controller chip containing control logic designed to complement the 8088 processor on an IBM PC compatible CPU. The chip replaces the following components:

<u>Qty.</u>	<u>Type</u>		<u>Description</u>
1	8255A-5	40 pin	Programmable Peripheral Interface
2	74LS244	20 pin	Octal Non-Inv Buffer
1	74LS240	20 pin	Octal Inv Buffer
1	74LS322	20 pin	8 bit Shift Reg
1	8284A	18 pin	Clock Generator + Driver
1	74LS157	16 pin	Quad 2 to 1 Mux
1	74LS155	16 pin	Quad 2 to 4 Decoder
1	74LS174	16 pin	Hex D - flipflops
2	74LS175	16 pin	Quad D - flipflops
1	Switch	16 pin	8 position
1	74LS280	14 pin	Parity Generator/checker
2	74125	14 pin	Quad Bus Buffer Gates
2	74LS74	14 pin	Dual D - flipflops
1	74LS32	14 pin	Quad 2 Input OR Gates
1	74LS30	14 pin	8 Input NAND Gate
1	74LS20	14 pin	Dual 4 Input NAND Gates
1	74LS10	14 pin	Triple 3 Input NAND Gates
1	74LS08	14 pin	Quad 2 Input AND Gates
2	74LS04	14 pin	Hex Inverters
1	74LS00	14 pin	Quad 2 Input NAND Gates

- 1 - 40 pin chip
- 4 - 20 pin chips
- 1 - 18 pin chip
- 6 - 16 pin chips
- 13 - 14 pin chips

Total Components Replaced 25

By utilizing the FE2000 you will:

- 1) lower assembly cost during manufacture
- 2) lower power requirements on the resultant board
- 3) attain higher quality and reliability due to having less total I. C. 's
- 4) reduce the size of a densely populated 4 layer board by at least 10 square inches.

C

Faraday CPU Controller—FE2000

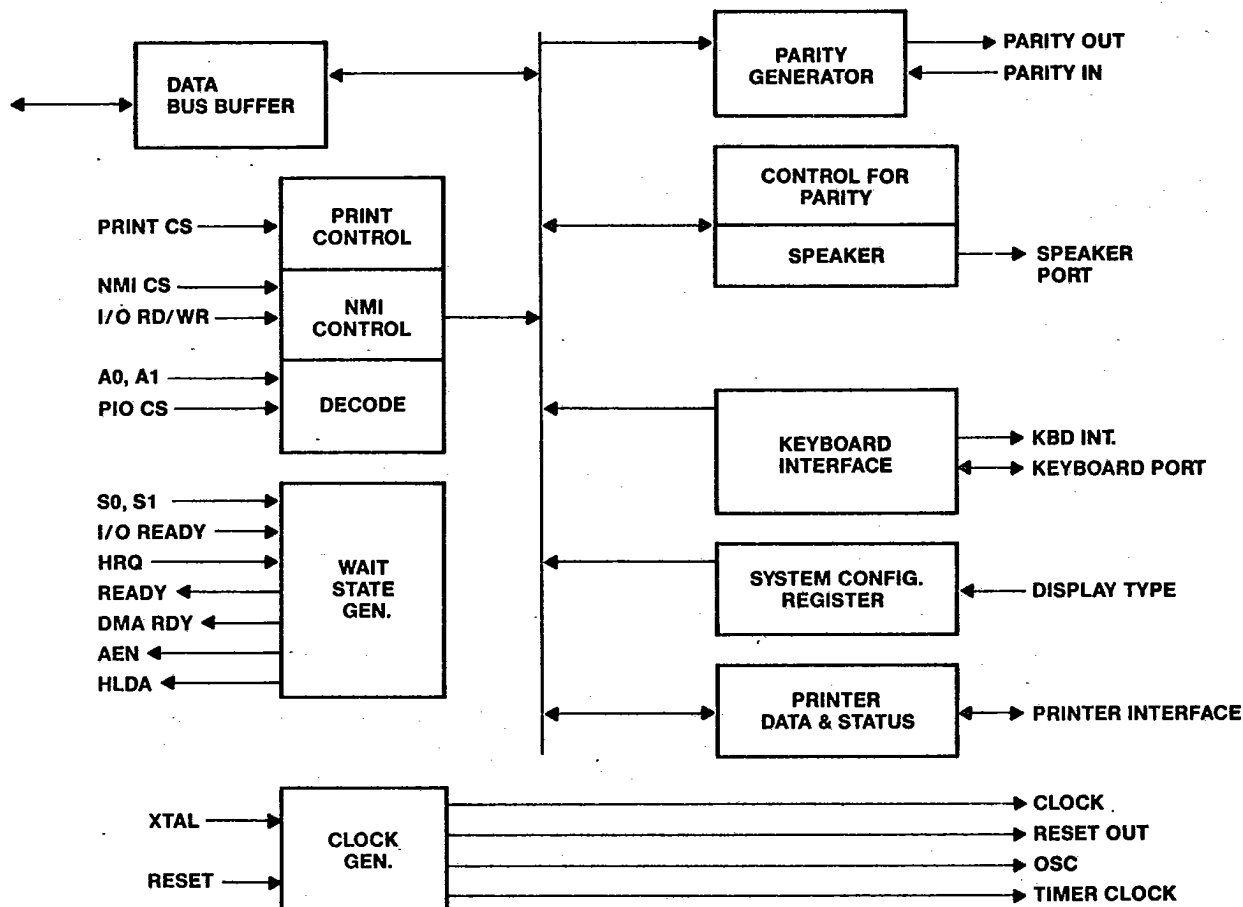
Features:

- Wait State Generator
- Enable/Disable NMI Control
- Parity Generator/Checker
- Internal System Configuration Eliminating External Switches
- Keyboard Scan Code and Interrupt Generator
- Parallel Interface to Printer (Centronics Interface)
- Clock Generator
- Uses a Crystal or a TTL Signal for Frequency Source
- Ready Synch Logic and System Reset Output
- 68 Pin Leaded Surface Mount Package
- CMOS
- Single +5 Volts Power Supply

The Faraday CPU Controller (FE2000) is a single chip with various control logic designed to complement the 8088 Processor to build an IBM compatible single board computer. The chip is packaged in a 68 pin J-type leaded surface

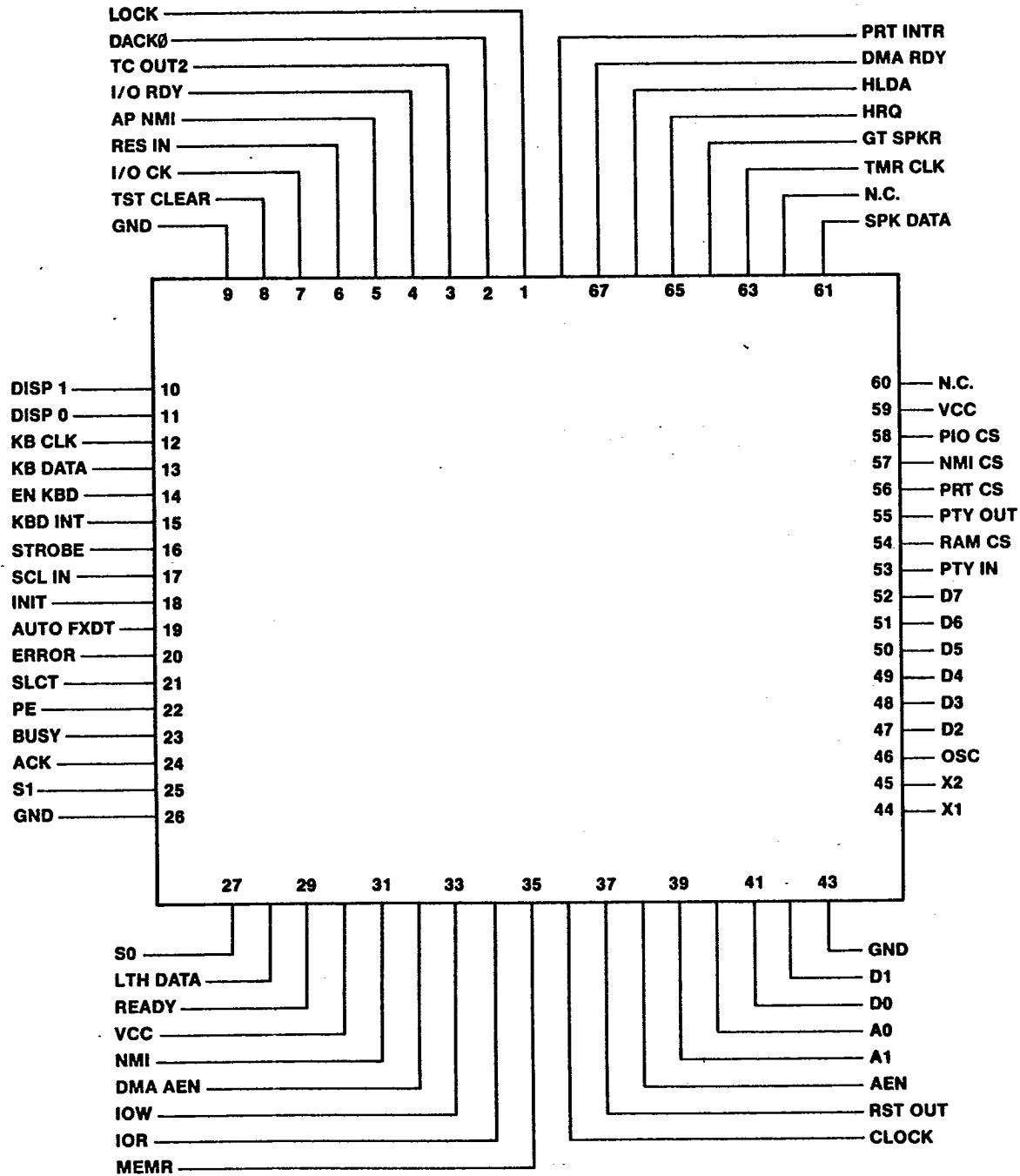
mount and uses HCMOS technology. A chip carrier socket for this plastic chip carrier is available from Burndy (Part #QILE6BP-408).

Figure: 1 FE2000 Block Diagram



Faraday CPU Controller—FE2000

Figure 2: Pin Diagram



Faraday CPU Controller—FE2000**Pin Description**

PIN	TYPE	SYMBOL	FUNCTION
1	I	LOCK	Lock from CPU
2	I	DACK 0	DMA acknowledge from DMA controller
3	I	TC OUT2	Timer 2 terminal count indicator
4	I	I/O RDY	To lengthen the I/O cycle for a slow memory or I/O device
5	I	AP NMI	NMI for 8087, if installed
6	I	RES IN	Reset in to generate reset out for processor and system
7	I	I/O CK	Error information on devices in the I/O channel
8	I	TST CLR	Externally tie to +5 volts through 4.7K OHM Resistor
9	—	GND	Ground
10	I	DISP 1	Display configuration Jumper 2
11	I	DISP 0	Display configuration Jumper 1
12	I	KB CLK	Clock from keyboard to recover data
13	I	KB DATA	Scan data from keyboard
14	O	EN KBD	Control line for keyboard clock
15	O	KBD INT	Keyboard Interrupt
16	O	STROBE	Strobe data to printer
17	O	SCL IN	Select to the printer
18	O	INIT	Reset to printer
19	O	AUTO FXDT	Auto paper feed to printer
20	I	ERROR	Error status from printer
21	I	SLCT	Select from printer
22	I	PE	Out of paper status from printer
23	I	BUSY	Busy from printer
24	I	ACK	Acknowledge from printer
25	I	S1	CPU status line S1
26	—	GND	Ground
27	I	S0	CPU status line S0
28	O	LTH DATA	Latch data to printer data port
29	O	READY	Synchronized ready to CPU
30	—	VCC	+5 volts power supply
31	O	NMI	Non-maskable interrupt to CPU
32	O	DMA AEN	Enable DMA to use CPU bus
33	I	IOW	I/O write from CPU control bus
34	I	IOR	I/O read from CPU control bus
35	I	MEMR	Memory read from CPU control bus
36	O	CLOCK	Clock output to CPU
37	O	RST OUT	Reset to 8088 and system
38	O	AEN	Control line to allow DMA channel to use data bus
39	I	A1	System address line A1
40	I	A0	System address line A0

Faraday CPU Controller—FE2000**Pin Description** (continued)

PIN	TYPE	SYMBOL	FUNCTION
41	I/O	D0	CPU data bus bit 0
42	I/O	D1	CPU data bus bit 1
43	—	GND	Ground
44	I	X1	Crystal input
45	O	X2	Crystal output
46	O	OSC	Output of the internal OSC. Its frequency is equal to that of the crystal.
47	I/O	D2	CPU data bus bit 2
48	I/O	D3	CPU data bus bit 3
49	I/O	D4	CPU data bus bit 4
50	I/O	D5	CPU data bus bit 5
51	I/O	D6	CPU data bus bit 6
52	I/O	D7	CPU data bus bit 7
53	I	PTY IN	Parity bit from parity RAM
54	I	RAM CS	RAM array chip select
55	O	PTY OUT	Parity bit to parity RAM
56	I	PRT CS	I/O port decode to select printer
57	I	NMI CS	Chip sel to NMI enable/disable latch
58	I	PIO CS	I/O port decode to keyboard, system configuration register and speaker ports
59	—	VCC	+5 volts power supply
60	—	N.C.	
61	O	SPK DATA	Data to speaker
62	—	N.C.	
63	O	TMR CLK	Clock signal to timer
64	O	GT SPKR	Gating to speaker data
65	I	HRQ	Hold request from DMA controller
66	O	HLDA	Hold ACK to DMA controller
67	O	DMA RDY	Wait state to DMA
68	O	PRT INTR	Interrupt request to CPU by printer

Faraday CPU Controller—FE2000

Programming:

The FE2000 accepts Read/Write commands initiated by the processor:

Write PIO Control Register

PIO CS	A1	A0	IOW
0	0	1	0

- D0 = +Gate speaker
- D1 = +Speaker data
- D2 = +Select system configuration switch low bits
- D3 = N/A
- D4 = -Enable RAM parity
- D5 = -Enable I/O check
- D6 = +Enable keyboard clock
- D7 = +Clear keyboard

Write Switch Register

PIO CS	A1	A0	IOW
0	1	0	0

- D0 = Number of floppy drives
- D1 = +8087 installed
- D2,D3 = System memory
- D4 = Display configuration Jumper 1 (DISP 1)
- D5 = Display configuration Jumper 2 (DISP 2)
- D6,D7 = Number of floppy drives.

Write PIO Configuration Lock Register:

PIO CS	A1	A0	IOW
0	1	1	0

- D0 = -Enable parity
- D1 = +8087 installed
- D2 thru D4 = Not used
- D5 = +Lock system switch register
- D6,D7 = Not used

Read PIO Control Register

PIO CS	A1	A0	IOW
0	0	1	0

Read KBD Scan Code

PIO CS	A1	A0	IOW
0	0	0	0

Read Switch Register

PIO CS	A1	A0	IOW
0	1	0	0

D0-D3 depends on PIO control register Bit 2
When PIO control register Bit 2 = 1

- D0 = Number of floppies.
- D1 = +8087 installed
- D2,D3 = System memory

When PIO control register Bit 2 = 0

- D0 = Display configuration Jumper 1
- D1 = Display configuration Jumper 2
- D2,D3 = Number of floppies

- D4 = +Timer 2 terminal count
- D5 = +Timer 2 terminal count
- D6 = +I/O CH check
- D7 = +PTY check

Printer Port Programming

PRINT CS	A1	A0	IOW	IOW	OPERATION
0	0	0	0	1	Read back printer data port
0	0	0	1	0	Write printer data port
0	0	1	0	1	Read printer status
0	0	1	1	0	N/A
0	1	0	0	1	Read back printer control port
0	1	0	1	0	Write printer control port
0	1	1	0	1	N/A
0	1	1	1	0	N/A

Read Printer Status Port Data Bit Definition:

- D0 thru D2 not used
- D3 = -Error
- D4 = +SLCT
- D5 = +Paper empty
- D6 = -ACK
- D7 = -Busy

Write Printer Control Port Data Bit Definition:

- D0 = -Strobe
- D1 = -Auto FDXT
- D2 = +Init
- D3 = -SCLT in
- D4 = +Printer interrupt enable

Faraday CPU Controller—FE2000

Temperature 0C to 70C

Supply Voltage

Minimum	Nominal	Maximum
4.75 V	5.00 V	6.00 V

All inputs and outputs are TTL compatible.

Signals	Minimum nsec	Timings Typical nsec	Maximum Maximum nsec
CLOCK high	75	80	85
CLOCK low	125		135
CLOCK period		210	
CLOCK rise time			10
CLOCK fall time			10
CLOCK ↘ to RESET ↘	8	13	19
CLOCK ↘ to READY ↗	-4	-5	-9
CLOCK ↘ to READY ↘	-6		-10
OSC ↘ to CLOCK ↗	6	8	15
OSC ↘ to CLOCK ↘	12	13	28
IOR or IOW ↘ to DMA RDY ↘	26	33	57
PRINT CS ↘ to LTH PRT ↘	54	66	108
PRINT CS ↗ to LTH PRT ↗			20
D0-D7 in to PTY OUT	30	41	69
IOR ↘ to DMA RDY ↘			57
IOW ↘ to DMA RDY ↘			57
MEMR ↘ to DMA RDY ↘			71

Faraday CPU Controller—FE2000

CPU Control

