UMC

T-52-33-15

UMC

UM82C088

PRELIMINARY

PC/XT Integration Chip

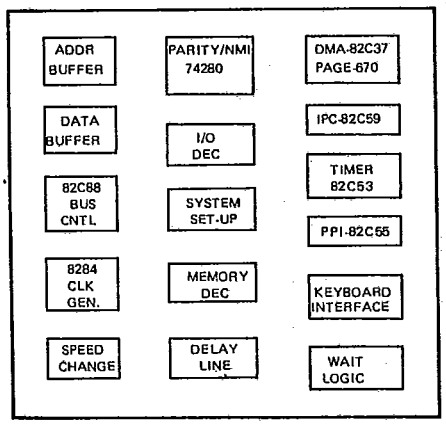
Features

- Fully IBM-PC/XT compatible
- 82C84 Clock generator with 2 clock-inputs to generate the CPU clock. These are 14.318 MHz and 30 MHz which will support 4.77 MHz and 10 MHz CPU clocks with 1/3 duty cycle.
- 82C88 Bus Controller
- 82C37 4 channel DMA controller, channel 0 is used for DRAM refresh
- 82C59 8 channel interrupt controller, level 0 is used for system time base, and level 1 for keyboard input
- 82C53 3 channel timer, channel 0 is used for system time base, channel 1 for DRAM refresh, and channel 2 for speaker audio
- 82C55 Peripheral I/O, used for keyboard interface and system configuration switch (same as the PC/XT)
- 74322 Keyboard interface, supports PC/XT type keyboard
- 74280 Parity check and generator
- 74670 4 bit page register for DMA
- Wait state logic
- NMI control logic
- ROM decoder for one 2764 and one 27256
- RAM decoder for 4164 or 41256 DRAM
- H/W and S/W CPU speed change and indicator
- Built-in delay line for RAS, CAS
- Low power consumption: less than 300 mW at 10 MHz CPU speed
- Small PCB size: 100 pin plastic Flat package

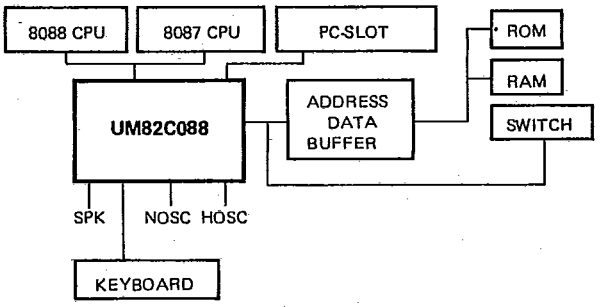
General Description

The UM82C088 is an IC specifically designed to function as the peripheral controller for 8088 microprocessors in an IBM PC/XT compatible computer. It is implemented in 1.5μ CMOS technology and is packaged in a 100 pin plastic flat package.

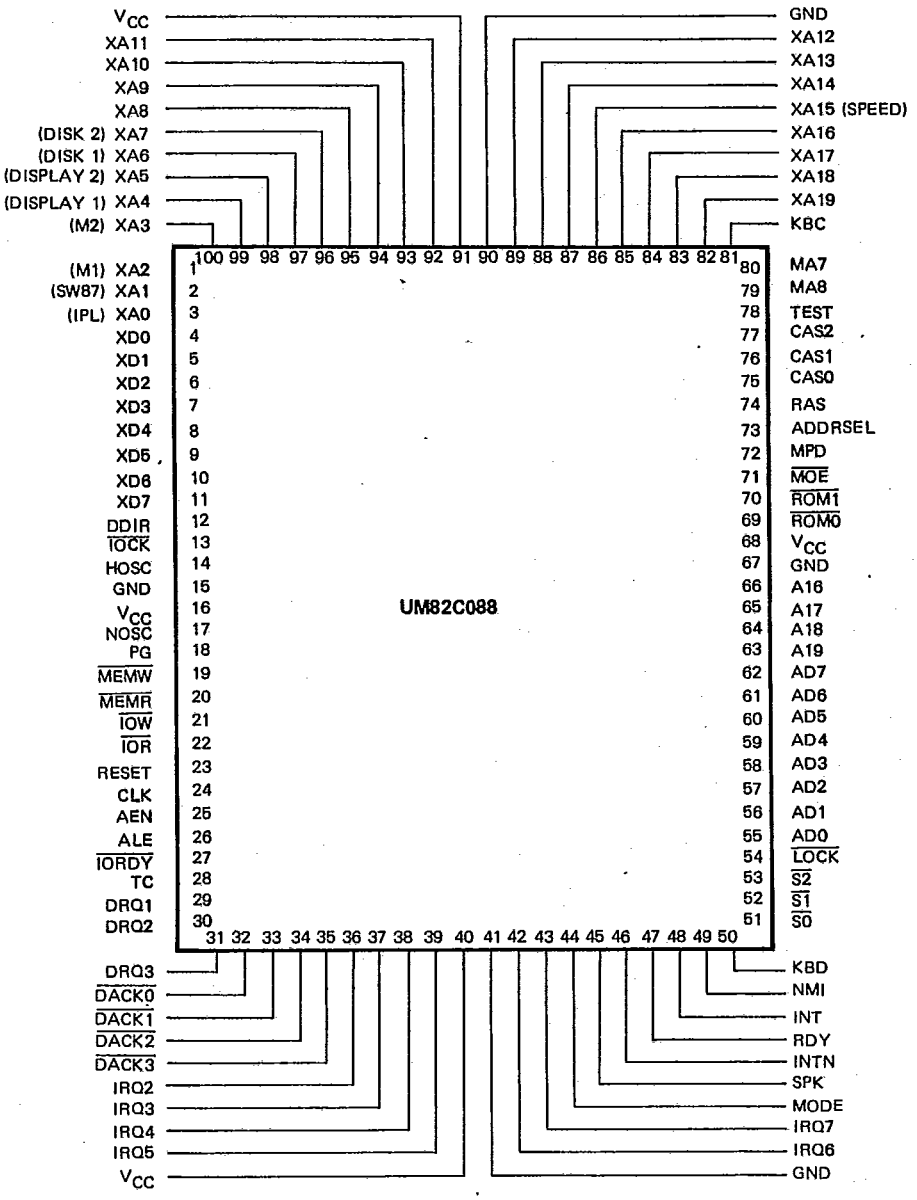
Block Diagram



System Configuration



Pin Configuration



PC Mainboard

Pin Description

Pin No.	Symbol	I/O	Description
17	NOSC	I	The clock input pin to which a 14.318 MHz clock is attached. The frequency is 3 times the CLK frequency in 4.77 MHz mode.
14	HOSC	I	The 2nd clock input pin to which a high speed clock is attached (max frequency = 30 MHz). The oscillator frequency is 3 times the CLK frequency during high speed mode.
24	CLK	O	The clock output signal used by the 8088 CPU. The frequency of this line is 1/3 duty cycle of NOSC or HOSC, depending on which speed mode is selected.
18	PG	I	Power-Good is an active high input signal which is used to generate the RST output. An RC connection can be used to establish a power up reset of proper duration.
23	RST	O	Reset, an active high output signal which is used to reset the CPU and system. Its timing characteristics are determined by pin PG.
22	$\overline{IOR}$	O	This command output line instructs an I/O device to transmit its data on to the data bus. It is supported by the internal 82C88 during the CPU cycle or the internal 82C37 during the DMA cycle. This signal is active low.
21	$\overline{IOW}$	O	This command output line instructs an I/O device to read the data on the data bus. It is supported by the internal 82C88 during the CPU cycle or the internal 82C37 during the DMA cycle. This signal is active low.
20	$\overline{MEMR}$	O	This command output line instructs the memory to drive its data onto the data bus. It is supported by the internal 82C88 during the CPU cycle or the internal 82C37 during the DMA cycle. This signal is active low.
19	$\overline{MEMW}$	O	This command output line instructs the memory to record the data present on the data bus. It is supported by the internal 82C88 during the CPU cycle or the internal 82C37 during the DMA cycle. This signal is active low.
26	ALE	O	Address latch enable. This output signal serves to strobe the address from CPU into the address latch. This signal is active high.
25	AEN	O	Address enable output. Used to control the system bus for the CPU or DMA. When high, the DMA controller has control of the address bus, data bus and command lines.
51 ⋮ 53	$\overline{S0}$ ⋮ $\overline{S2}$	I	Status input pin from the CPU. The internal 82C88 decodes these inputs to generate command and control signals at the appropriate times.
54	$\overline{LOCK}$	I	Input pin that indicates that the internal 82C37 is not to gain control of the system bus while lock is active low.
49	NMI	O	Non-maskable interrupt. An edge trigger (a transition from low to high) output to the 8088 CPU which causes a type 2 interrupt. (a transition from low to high). There are three different sources to generate NMI: one is input from lock, the others are internal parity check logic and INTN input.

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
48	INT	O	Interrupt output, this pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU and is generated from internal 82C59.
46	INTN	I	Input from external 8087 NPX to generate an NMI output to indicate an error condition of 8087.
47	RDY	O	Ready output. This output acknowledges the internal wait logic or $\overline{\text{IORDY}}$ input pin, which will complete the data transfer. This signal is active high.
27	$\overline{\text{IORDY}}$	I	Input signal used to insert wait state into CPU & DMA bus cycles.
71	$\overline{\text{MOE}}$	O	Output signal used to enable the external memory buffer, which is selected by internal memory decoder logic ($\overline{\text{ROM0}}$-$\overline{\text{ROM1}}$ & CAS0-CAS2). This line is active low.
12	DDIR	O	Output signal which controls the direction of pins XD0-XD7. A high on this line indicates data from system to chip, and low on this line indicates data from chip to system.
74	RAS	O	Memory column address, active high.
75 ⋮ 77	CAS0 ⋮ CAS2	O	Generated by internal memory decoder logic to strobe DRAM column address, address range from 00000H to 9FFFFH, total 3 banks for 256KB DRAM (max. 640KB). These signals are active high.
73	ADDRSEL	O	Address select used to select the DRAM row-address or column-address. A high indicates the row address has been selected and a low indicates the column address is enabled.
79 80	MA8 MA7	O	Provides DRAM chips MA7, MA8 address lines. First cycle is row-address and second cycle is column address and refresh cycle address.
72	MPD	I/O	Memory parity data. Inputs when $\overline{\text{MEMR}}$ is active, and outputs when $\overline{\text{MEMW}}$ is active. Used for internal parity-check logic.
69 70	$\overline{\text{ROM0}}$ $\overline{\text{ROM1}}$	O	Generated by internal memory decoder logic to enable the external EPROM chips. Address Ranges from F6000H to FFFFFH max, to select two 27256s or one 2764 and one 27256. These lines are active low.
55 ⋮ 62	AD0 ⋮ AD7	I/O	Address/Data bus. These eight lines constitute the time in multiplexed memory/IO address & data buses, which are connected directly to the 8088 CPU AD0-AD7 bus.
66 ⋮ 63	A16 ⋮ A19	I	Address bus. These are the four most significant address lines for memory/IO operations and are connected directly to the 8088 CPU A16/S3-A19/S6 bus.
3 ⋮ 1 100 ⋮ 96	XA0 ⋮ XA7	I/O	Address bus. Comes from system buses AD0-AD7 which are internally latched by ALE during the CPU-Cycle, and are supported by the internal 82C37 during the DMA-Cycle.

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
85 ⋮ 82	XA16 ⋮ XA19	O	Address bus comes from system buses A16-A19 which are outputs only.
4 ⋮ 11	XD0 ⋮ XD7	I/O	Data bus outputs when the CPU write is active from the system bus AD0-AD7. Inputs when the CPU read is active or during the DMA cycle.
95 ⋮ 92 89 ⋮ 86	XA8 ⋮ XA15	I/O	Address pins A8 through A15 are Bi-directional and are supported by the external 8088 CPU A8-A15 bus during the CPU cycle, and by the internal 82C37 during the DMA cycle.
36 ⋮ 39 42 ⋮ 43	IRQ2 ⋮ IRQ7	I	These six input-only signals are used to generate interrupt requests to the CPU from the internal 82C59. IRQ2 is highest priority and IRQ7 the lowest. A rising-edge signal will generate an INT output to the CPU if the level of the 82C59 is not masked.
29 ⋮ 31	DRQ1 ⋮ DRQ3	I	These three lines are active-high input-only lines used by the peripherals to request DMA cycles, which are connected to the internal 82C37.
32 ⋮ 35	$\overline{\text{DACK0}}$ ⋮ $\overline{\text{DACK3}}$	O	These four signals are low-level active output-only signals issued by the internal 82C37 to indicate that the corresponding DRQ has been honored and the 82C37 will take the bus and proceed with the requested DMA cycle.
28	TC	O	Terminal count. This signal is an output-only active high signal issued by the internal 82C37. It indicates that one of the DMA channels has reached its preprogrammed number of transfer cycles.
13	$\overline{\text{IOCK}}$	I	This is a low-level input-only signal used to report error conditions on the bus-attached interface circuits. This signal when set low, will generate a NMI output.
81	KBC	I/O	Keyboard clock. When pulled low by internal logic, will reset the external keyboard. Otherwise the clock generated by the external keyboard is used as data.
50	KBD	I/O	Keyboard data. When pulled low from internal logic KBD will reset the external keyboard, or a serial data transmitting line from the keyboard to the internal logic, which is SYNC'd with the keyboard clock.
45	SPK	O	Generated from the internal 82C53. Can generate a programmable frequency output to drive an external AMP for a speaker.
44	MODE	O	Speed indicator. A high on this line indicates the CPU is working in high speed mode, a low on this line indicates the CPU is working in 4.77 MHz mode.

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
16 40 68 91	VCC	–	Power supply.
15 41 67 90	GND	–	Ground
78	TEST		This pin is provided for TEST only.

Set Up Descriptions

The following set up signals are multiplexed inputs with XA bus, but only available during RST active.

(a) Set up Pin Description

Pin No.	Symbol	I/O	Description
3	IPL	I/O	82C55 port C-BIT 0, during port B-BIT 3 = 0.
2	SW87	I/O	82C55 port C-BIT 1, used to decide 8087 existence during port B-BIT3 = 0.
1 100	M1 M2	I/O	Memory size setting Port OEOH, Bit 4, 5.
99 98	DISPLAY1 DISPLAY2	I/O	82C55 port C-Bit 0, 1. Used to decide display card type during port B-Bit 3 = 1.
97 96	DISK1 DISK2	I/O	82C55 port C-Bit 2, 3. Used to decide disk number during port B-Bit 3 = 1.
86	HL	I/O	Select CPU speed, 1 = Low, 0 = High.

(b) Set up DIP-SW Description

SW NO	Description		ON	OFF	SW NO	Description		ON	OFF
SW-1		Speed	H1	L0	SW-5	6-ON	Disk	EGA	CGA
SW-2		8087	W/O	W		6-OF	Type	–	MGA
SW-3	4-On	Mem Size	640K	512K	SW-7	8-On	Disk No.	1 Disk	2 Disk
	4-Off		–	256K		8-Off		3 Disk	4 Disk

Functional Description

Clock Generator

The clock generator is the functional equivalent of an 82C84 generator. It also generates the clock for the timer.

Features:

- Generates system clock for the 8088.
- Frequency sources are TTL signals
- TTL outputs for peripheral devices.
- Power-up reset for the processor.
- READY synchronization.

Bus Controller

The bus controller is the functional equivalent of an 8288 for CPU bus operations, and generates the bus controls for CPU operations.

Mode Controller

The system clock can be switched via either software or hardware:

Software user can write port $\phi C\phi H$ to select the system clock. A write command to this port will toggle CPU speed.

Hardware user can utilize a button key or a jumper to XA15 (HL) signal to select the appropriate mode during power on reset.

Each switching manner is independent of the other. Hardware setting is recognized only when RST is active, after then the system clock can be switched only by software.

Wait State Generator

When system clock is running at 4.77 MHz, the wait state generator generates one wait state on all CPU I/O and DMA operations. When system clock is 10 MHz, the wait state generator inserts 4 wait states on all CPU I/O operations and 1 wait state on all DMA operations. It also synchronizes the external ready (I/O CHRDY) that may be used to generate wait states for slower I/O devices.

No wait state is inserted for on-board memory access. When the system clock is running at the turbo rate (10 MHz) two wait states will be inserted for memory access on the expansion slots.

Inserted wait state:

	Low	High
Onboard Memory	0	0
Onboard I/O	1	4
Slot Memory	0	2
Slot I/O	1	4
DMA	1	1

DMA

The DMA (Direct Memory Access) is the functional equivalent of an 82C37 DMA controller. This function improves the microprocessor's system by allowing external devices to directly transfer information from the system memory. Channel 0 is reserved for the refresh of RAM memory.

Features:

- Address increment or decrement.
- Four independent DMA channels.
- Software DMA request. Enable/disable control of individual DMA requests. Independent autoinitialization of all channels.

Interrupt Controller

The programmable interrupt controller in the UM82C088 functions as a system-wide interrupt manager in a Turbo XT system, which is compatible to an Intel 82C59 interrupt controller. This function controls when and which I/O device is being serviced by the microprocessor in an efficient manner.

Features:

- Eight level priority controller.
- Programmable base vector address.
- Programmable interrupts modes (algorithms).
- Compatible with the 8088.

Timer

The timer is the functional equivalent of an 82C53 timer. Channel 0 is tied to interrupt 0, channel 1 is used to generate refresh, and channel 2 is used for the speaker port.

Features:

- Three independent 16-bit counters.
- Count binary or BCD.

PIO

The PIO is used for system configuration, to control the keyboard and speaker ports, and to enable error checks.

Keyboard Port

The keyboard port connects to an IBM compatible keyboard.

Parity Generator

The parity generator checks and generates even parity for RAM memory.

*Remarks:

(1) Port 0C0H: Write only.
A write command to this port will toggle CPU speed.

(2) Port 0E0H: Status Read only.

Bit 4	Bit 5	Bit 6	Bit 7
M1	M2	X	Speed mode

Memory Size.
11: 256KB
01: 512KB
-0: 640KB

0 Low
1 High

Programming

The UM82C088 accepts I/O read/write commands from the CPU.

I/O Address Map

Address	Definition
000H-01FH	DMA Contoller (82C37)
020H-03FH	Interrupt Controller (82C59)
040H-05FH	System Timer (82C53)
060H-07FH	Parallel port (82C55)
080H-09FH	DMA Page Register (74670)
0A0H-0BFH	NMI Mask Register
0C0H-0C3H	Change Speed
0E0H-0E3H	Status

The timer is programmed the same as the 82C53 timer, the DMA controller is programmed the same as the 82C37 DMA controller, and the interrupt controller is programmed the same as the 82C59 interrupt controller.

PIO

The PIO is the equivalent of the 82C55 PIO, but it is configured in a fixed way for system configuration, controling the speaker port, and the keyboard port.

Keyboard Data Register

The keyboard data register is a read only register that is used to read data from the keyboard. When a character is in the register, interrupt 1 will be sent to the interrupt controller. The register may be cleared by setting bit 7 of the PIO register.

DC Electrical Characteristics (V_{CC} = 4.75 to 5.25V, T_A = 0 to 70°C)

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{IL}	Input Low Voltage	-0.3	+0.8	V	
V_{IH}	Input High Voltage	+2.2	V_{CC}+0.3	V	
V_{OL}	Output Low Voltage		+0.4	V	I_{OL} = 4.0 mA
					I_{OL} = 16.0 mA (K_{BC}, K_{BD}, M_{PD} only)
V_{OH}	Output High Voltage	+3.0		V	I_{OH} = -2.0 mA
					I_{OH} = 8.0 mA (M_{PD} only)
V_{IHR}-V_{ILR}	PG Input Hysteresis	0.25		V	
I_{CC}	Operating Supply Current		50	mA	

AC Characteristics (V_{CC} = 4.75 to 5.25V, T_A = 0 to 70°C, C_L = 20pF)

Symbol	Parameter	Normal Speed		High Speed		Unit
		Min.	Max.	Min.	Max.	
T1	Input clock period	70		30		ns
T2	Input clock high time	25		12		ns
T3	Input clock low time	25		12		ns
T4	Input clock rising/falling time		3		3	ns
T5	CPU CLK High time	75	82	38	45	ns
T6	CPU CLK Low time	125	133	53	61	ns
T7	CPU CLK cycle period	210		100		ns
T8	High speed mode change to low speed mode CLK high time	110	180			ns
T9	Low speed mode change to high speed mode CLK high time			110	140	ns
T10	RDY delay time	–10	0	–10	0	ns
T11	ALE active delay time (from status)	4	20	4	20	ns
T12	ALE inactive delay time (from CLK)	0	15	0	15	ns
T13	Command active delay time (from CLK)	0	15	0	15	ns
T14	Command inactive delay time (from CLK)	0	15	0	15	ns
T15	Status inactive setup time	35		35		ns
T16	Address (AD0–AD7, XA8–XA15, A16–A19) valid to $\overline{MOE}$ active/inactive delay		40		40	ns
T17	Command active/inactive to RAS active/ inactive, MEM READ cycle		6		6	ns
	Command active to RAS active, MEM WRITE cycle	37	76	20	39	ns
	Command inactive to RAS inactive, MEM WRITE cycle	2	41	2	24	ns
T18	Command active to ADDRSEL active delay, MEM READ cycle	36	73	19	36	ns
	Command active to ADDRSEL active delay, MEM WRITE cycle	106	143	52	69	ns
T19	Command inactive to ADDRSEL inactive delay, MEM READ cycle	36	73	19	36	ns
	Command inactive to ADDRSEL inactive delay, MEM WRITE cycle	71	108	34	54	ns
T20	Command active to CAS active delay, MEM READ cycle	106	145	52	71	ns
	Command active to CAS active delay, MEM WRITE cycle	176	215	83	105	
T21	Command inactive to CAS inactive delay, MEM READ cycle		8		8	ns
	Command inactive to CAS inactive delay, MEM WRITE cycle	2	43	2	26	ns

PC Mainboard

AC Characteristics (Continued)

Symbol	Parameter	Normal Speed		High Speed		Unit
		Min.	Max.	Min.	Max.	
T22	Command to $\overline{MOE}$ delay (ROM cycle)		12		12	ns
T23	Command to $\overline{ROM}$ delay		12		12	ns
T24	XD to AD bus delay		40		40	
T25	Read data hold time	10		10		ns
T26	Command inactive to AD0–AD7 output floating	35		30		ns
T27	Command active to AD0–AD7 active	95	180	23	105	ns
T28	Command active to data valid for on board IOR	115	210	43	135	ns
T29	AD to XD bus, MPD active		40		40	ns
T30	AD to XD bus, MPD inactive delay		40		40	ns
T31	Address setup time	30		30		ns
T32	Address hold time	25		25		ns
T33	CLK to DDIR delay		50		50	ns
T34	On board IOW data setup time	150		150		ns
T35	On board IOW data hold time	25		25		ns
T36	XA address to MA7, MA8 delay		40		40	ns
T37	ADDRSEL to MA7, MA8 delay		10		10	ns
T38	$\overline{DACKX}$ delay time (from DCLK Low)		170		170	ns
T39	AEN active delay time (from DCLK high)		140		140	ns
T40	AEN inactive delay time (from DCLK high)	110	140	100	220	ns
T41	XA15–XA0 active delay time (from DCLK high)		110		110	ns
T42	XA15–XA0 inactive delay time (from DCLK low)	110		100		ns
T43	$\overline{XA19}$–XA16 active delay time (from $\overline{DACKX}$ active)		40		40	ns
T44	XA19–XA16 inactive delay time (from DCLK low)	110		100		ns
T45	DMA read command active delay time from DCLK high)		150		150	ns
T46	DMA read command inactive delay time (from DCLK high)		145		145	ns
T47	DMA write command active delay time (from DCLK high)		150		150	ns
T48	DMA write command inactive delay time (from DCLK high)		115		115	ns
T49	DMA cycle DDIR delay time (from AEN)		40		40	ns
T50	TC delay time (from DCLK high)		40		40	ns

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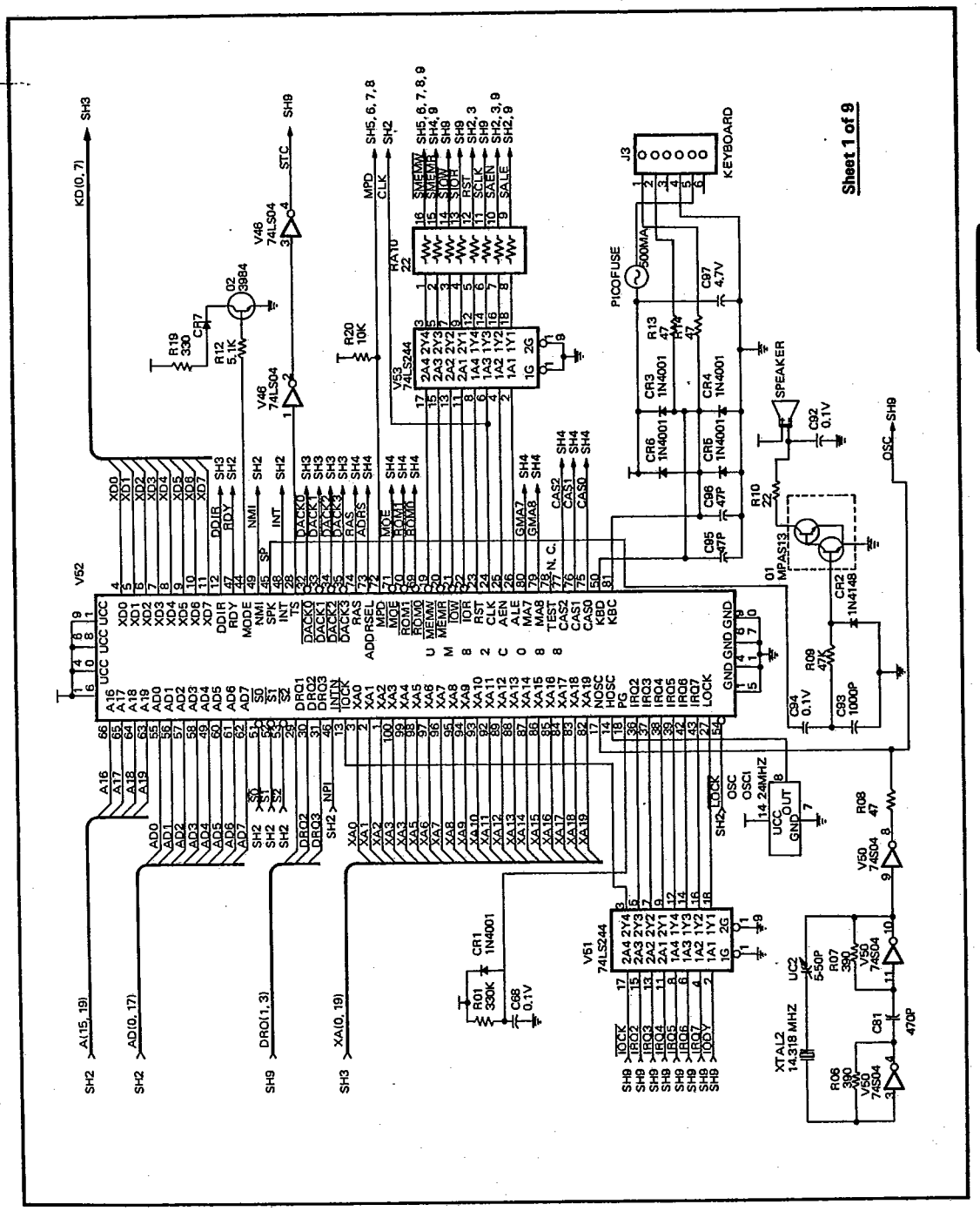
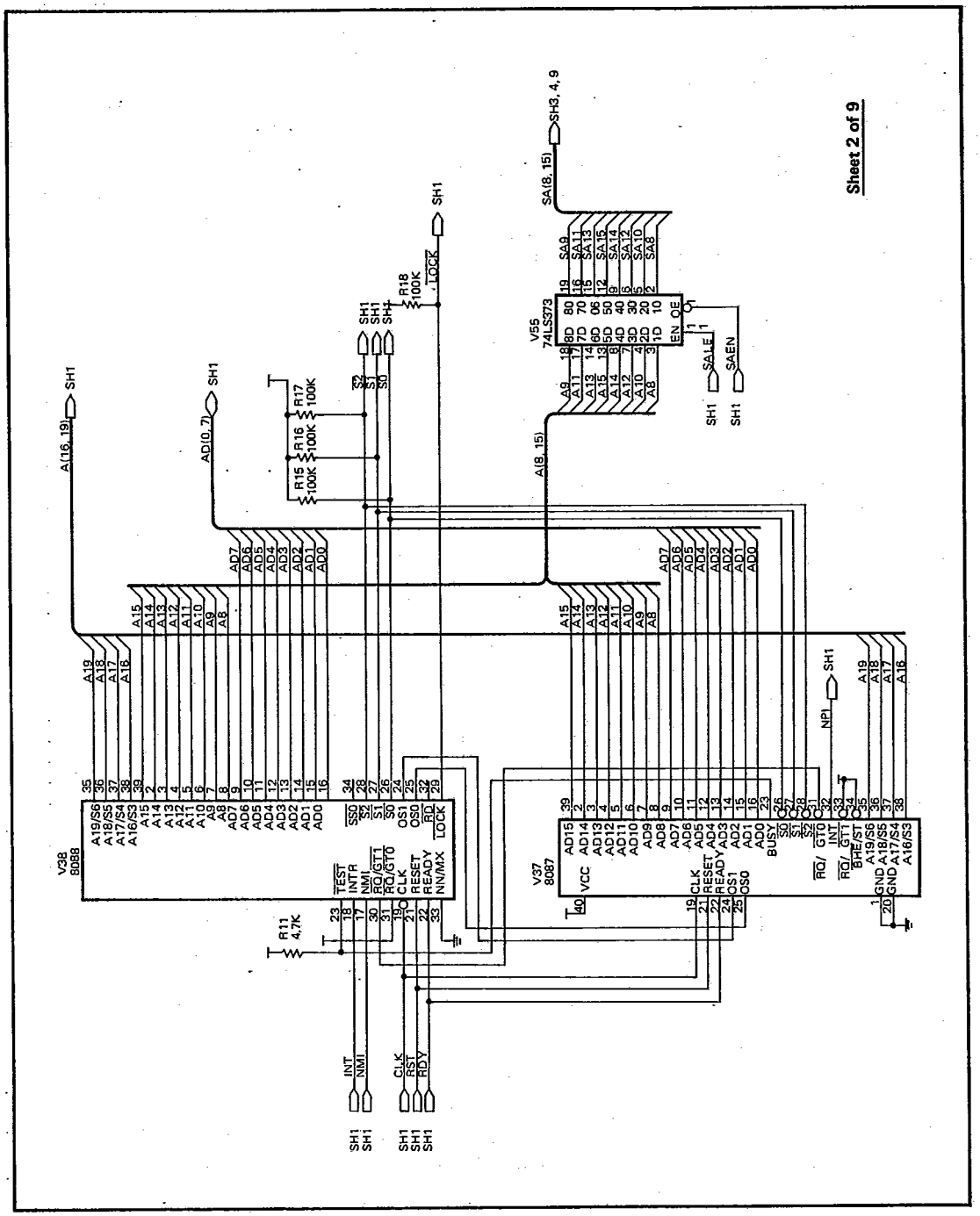
Application Circuits



Application Circuits (Continued)



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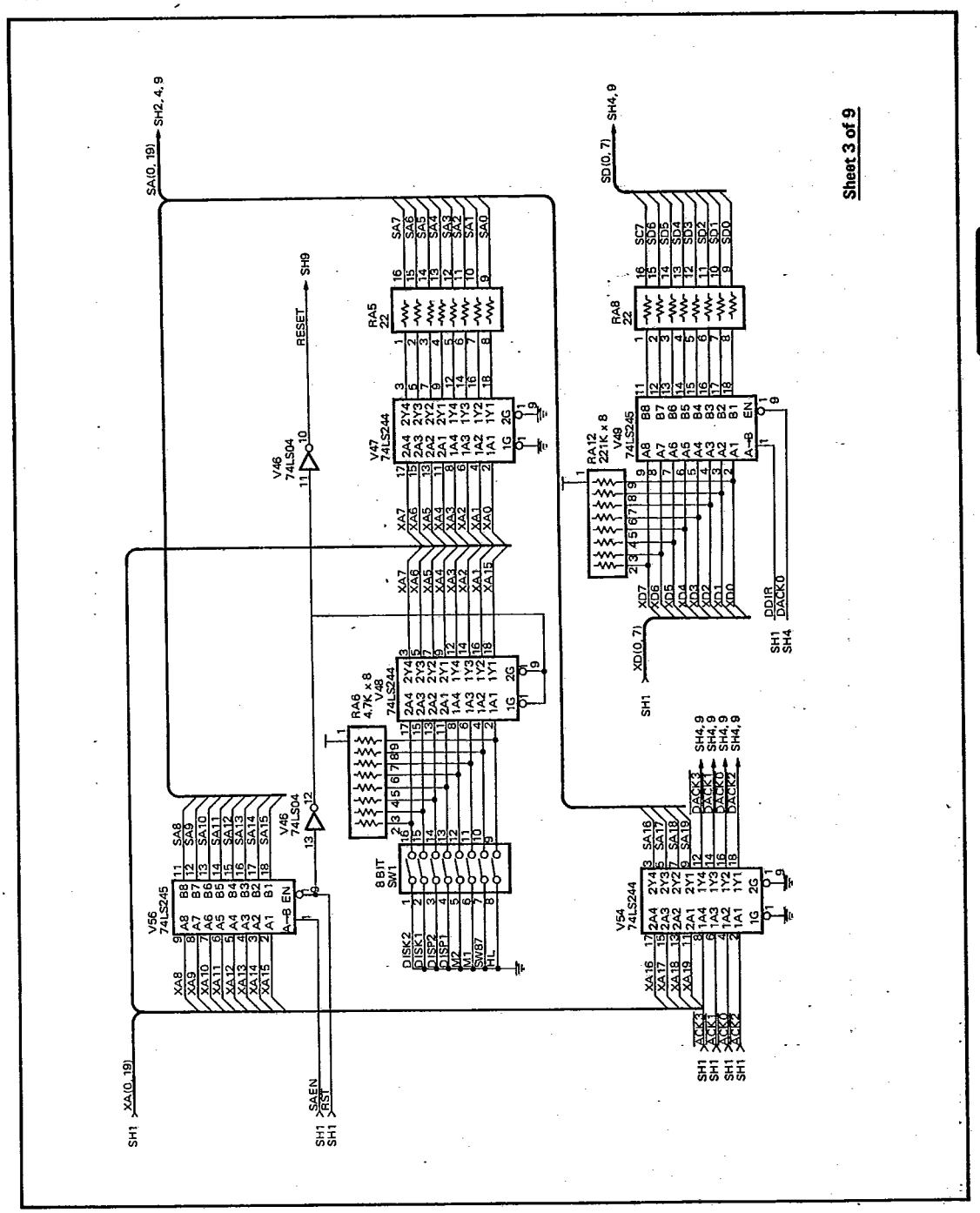

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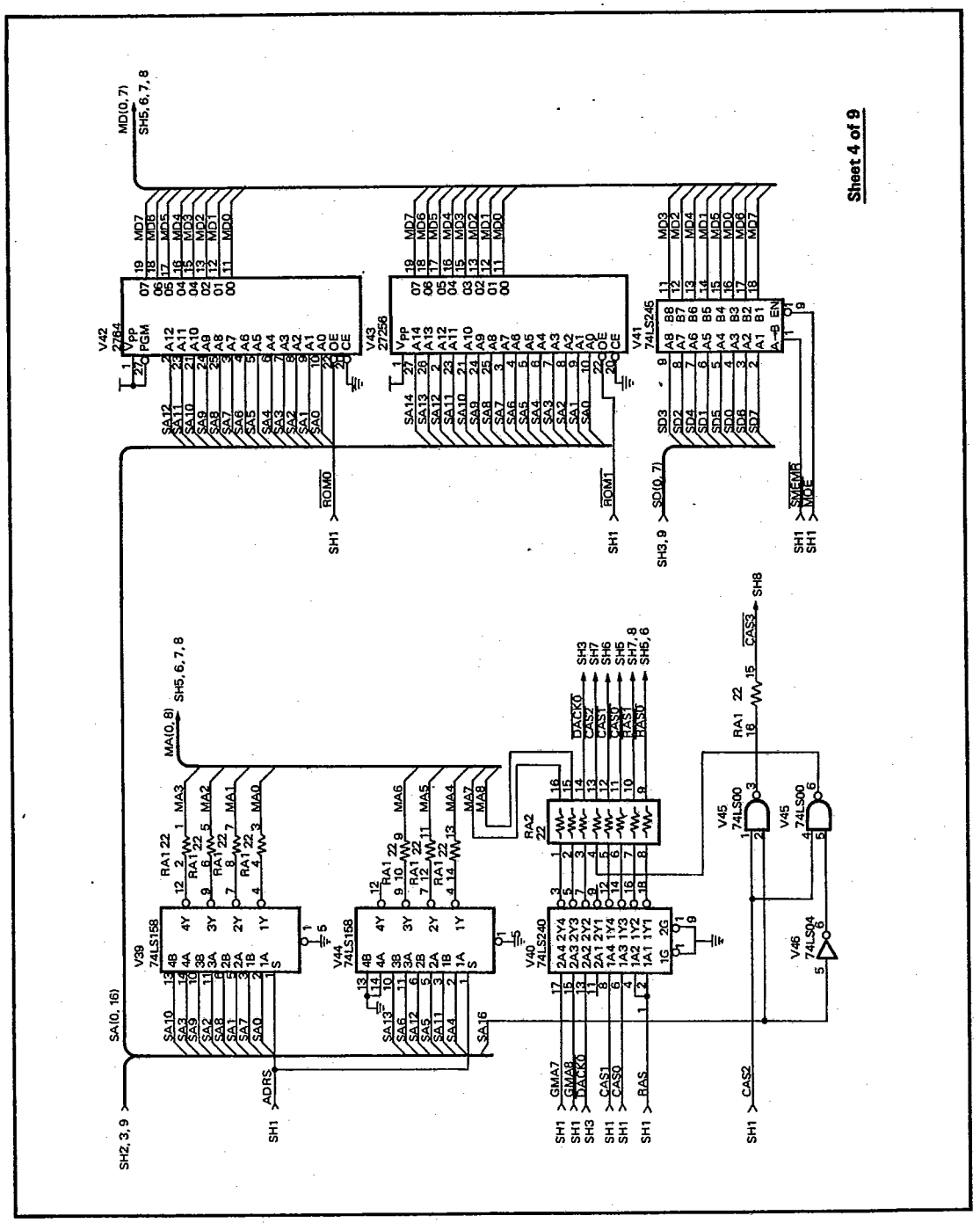

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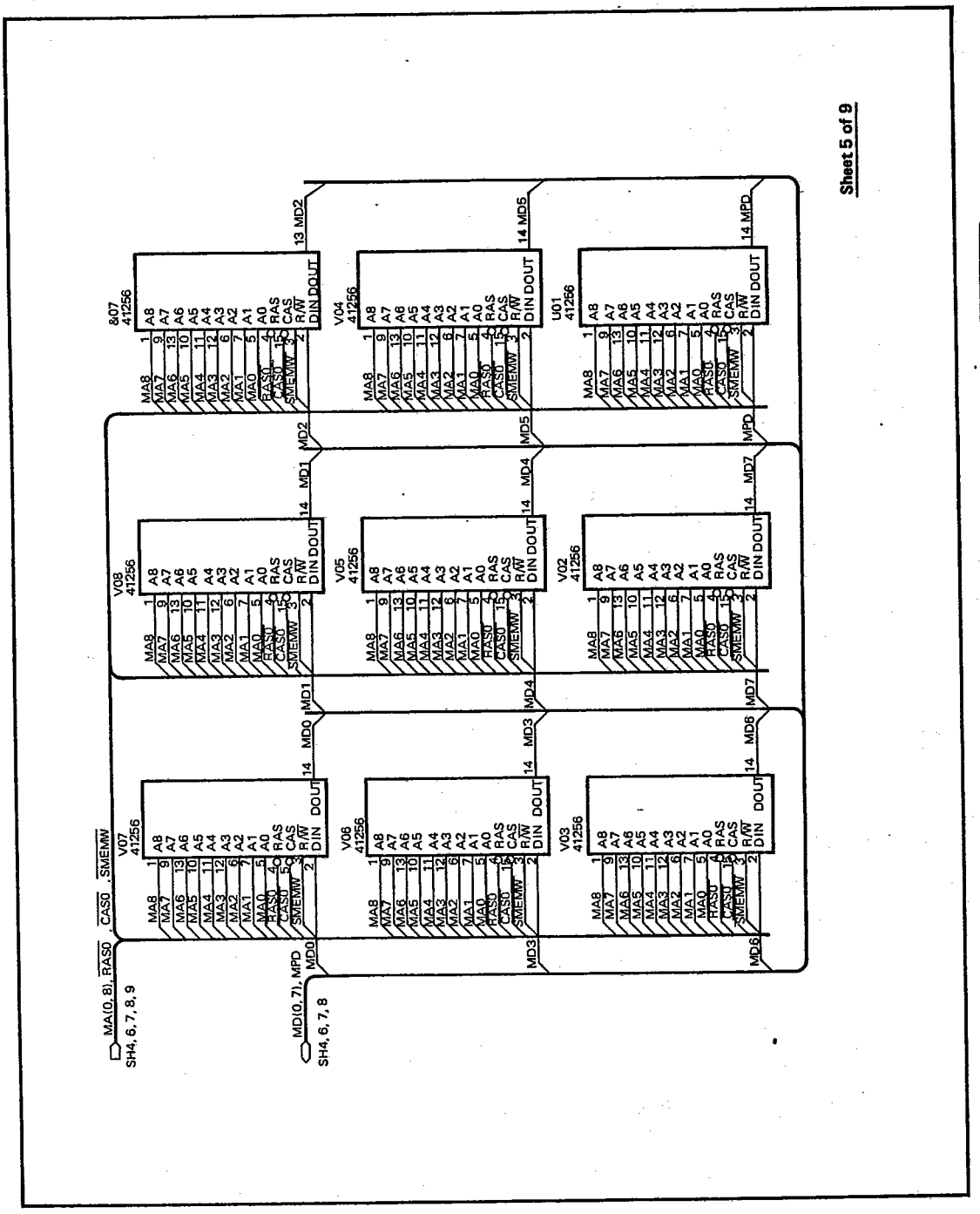

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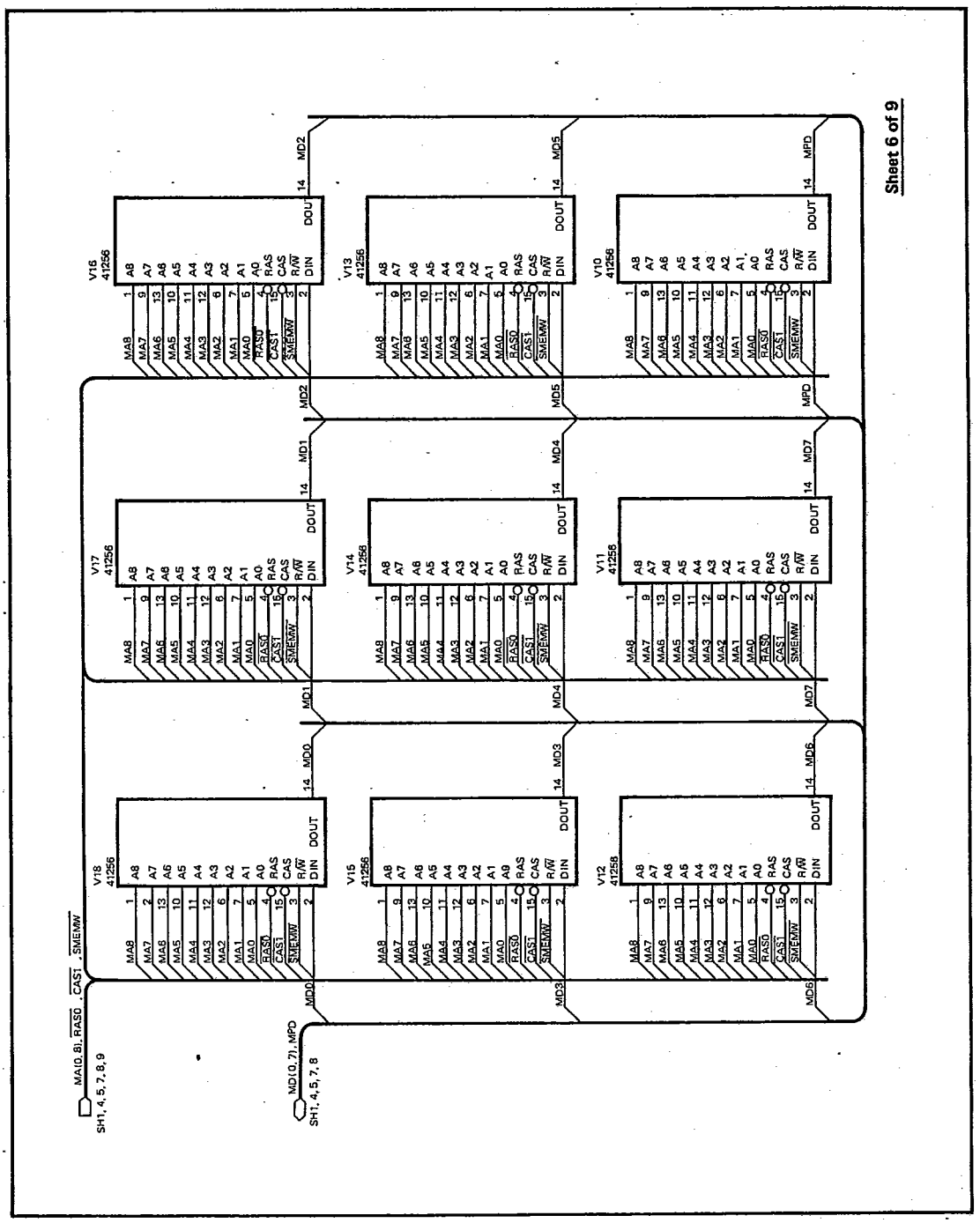

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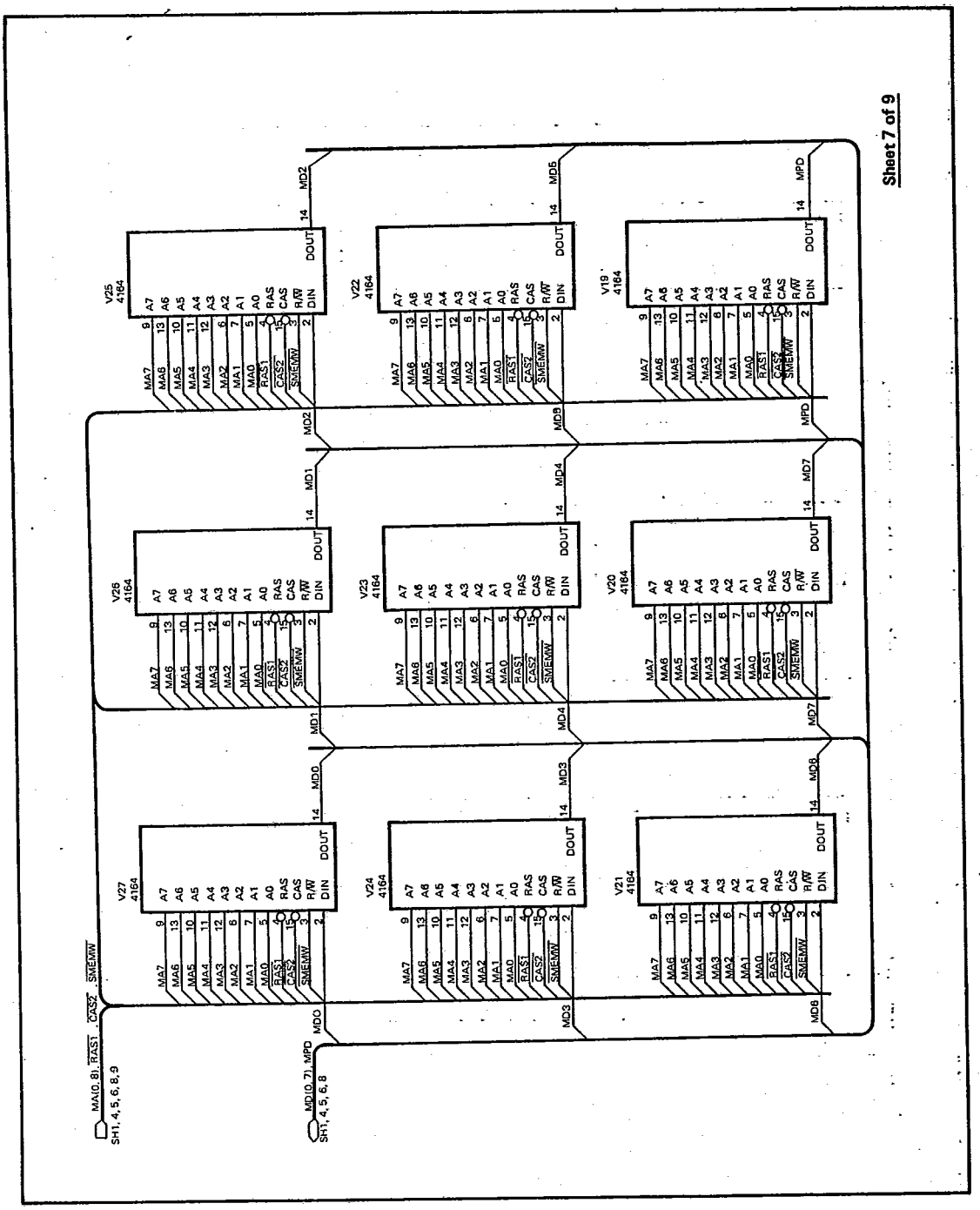

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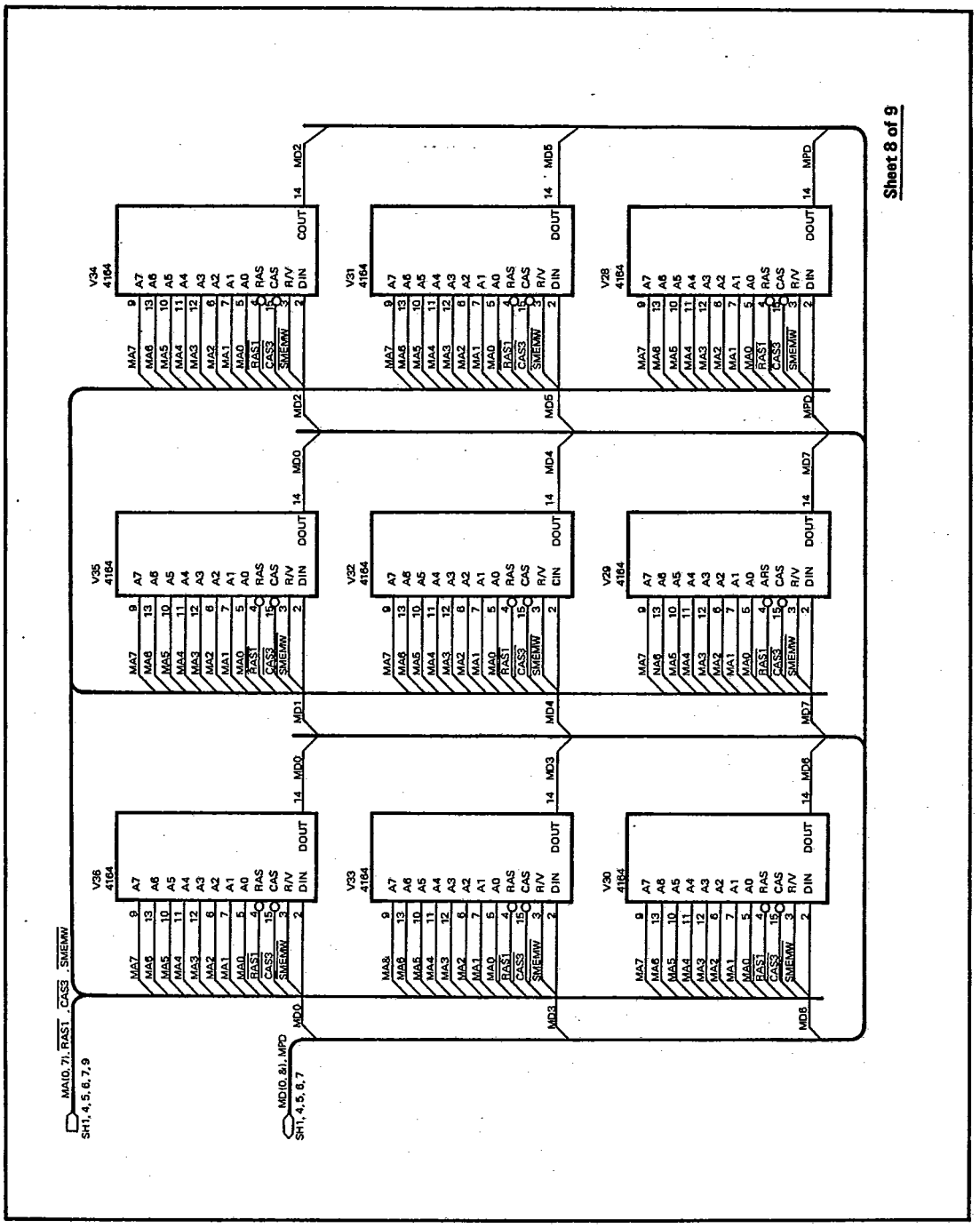

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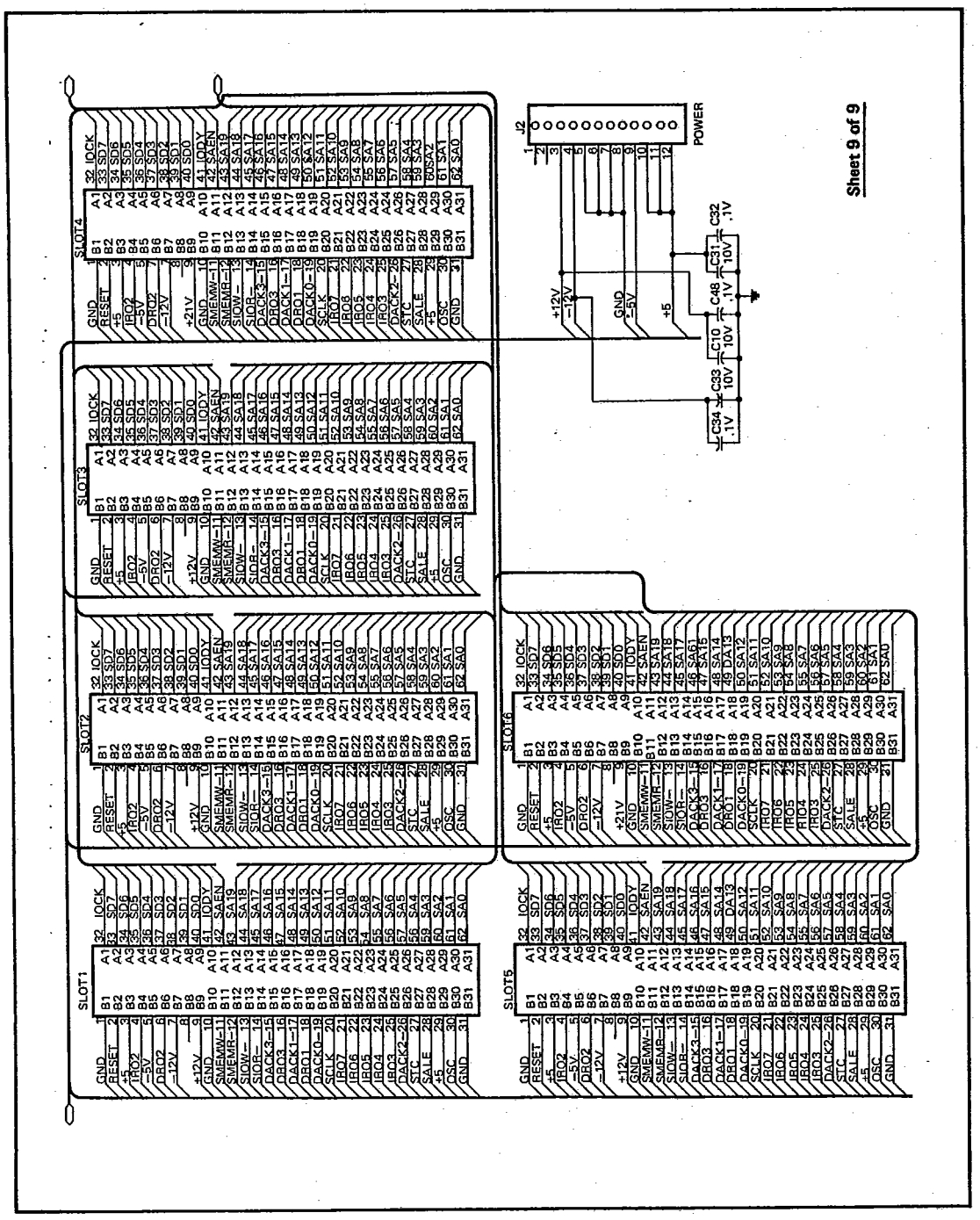
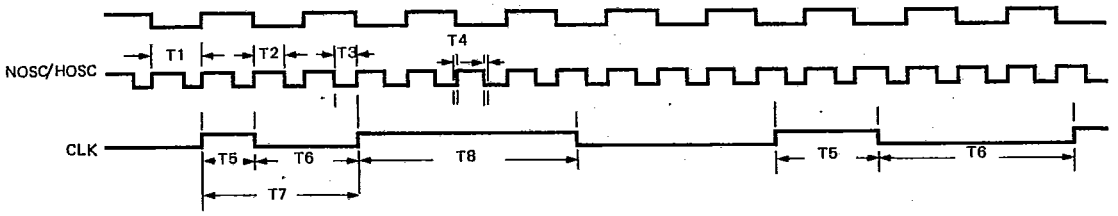
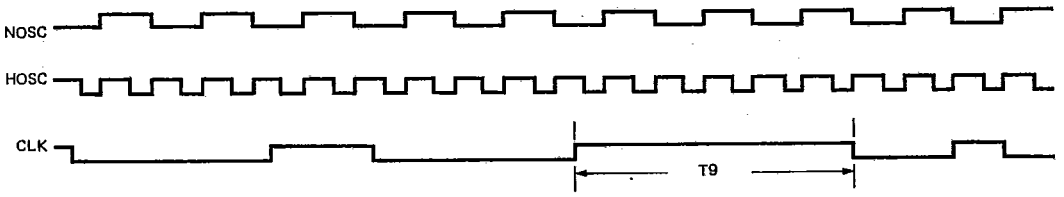


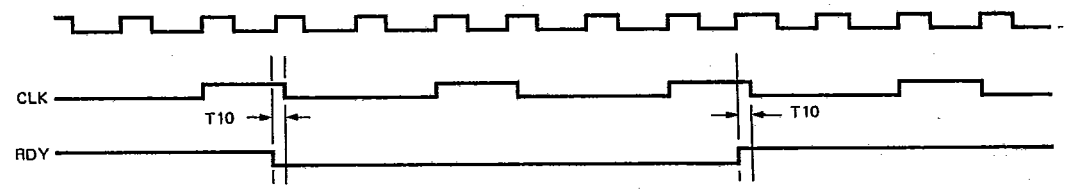
Timing Waveforms



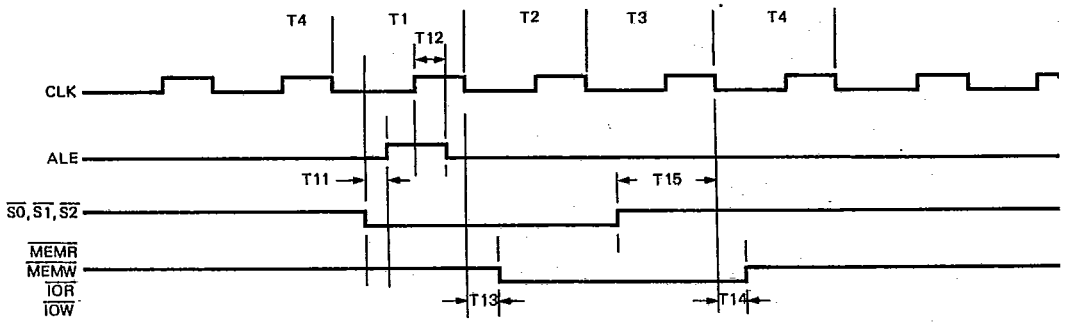
High Speed Change to Low Speed



Low Speed Change to High Speed



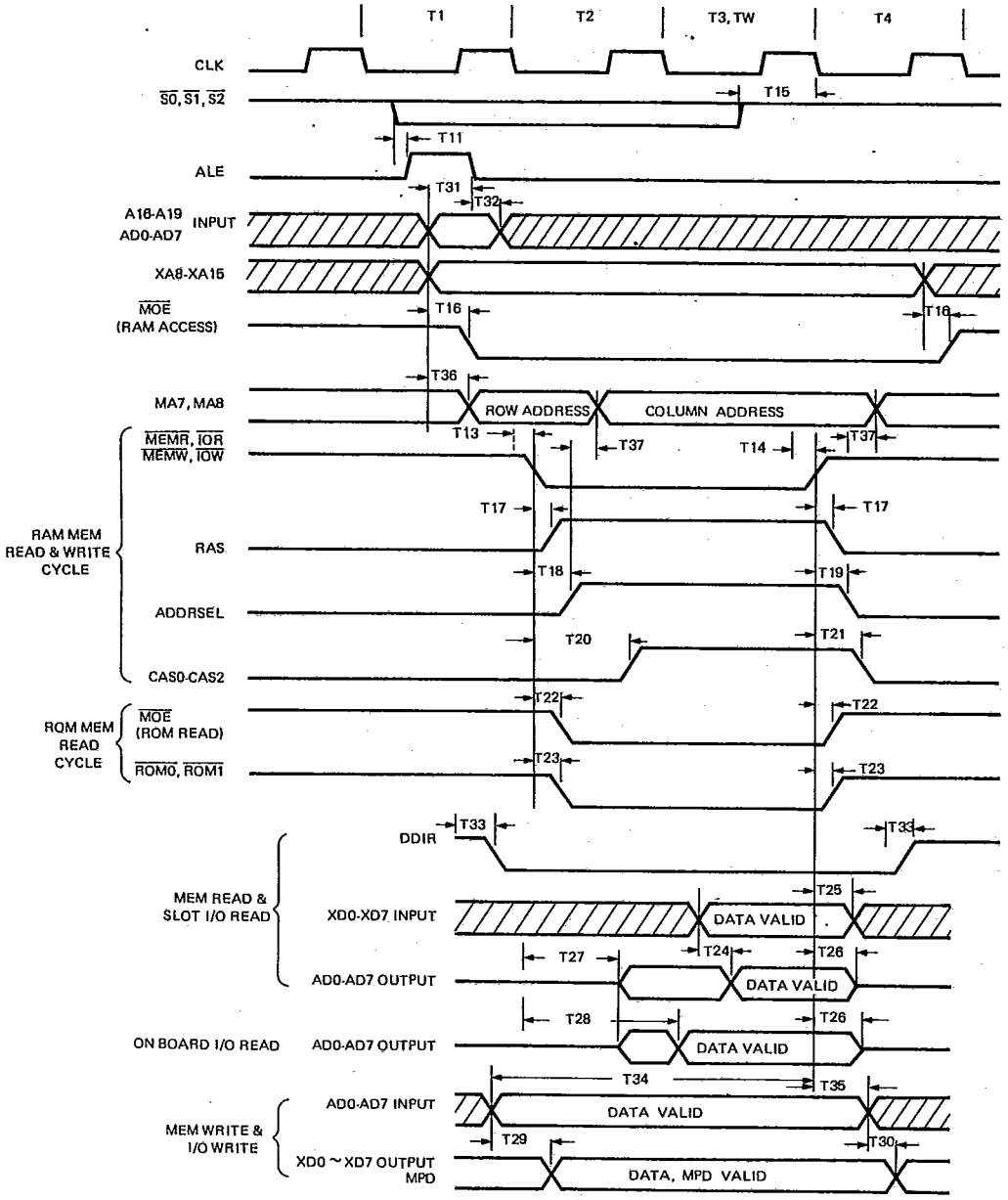
RDY TIMING



CPU Timing

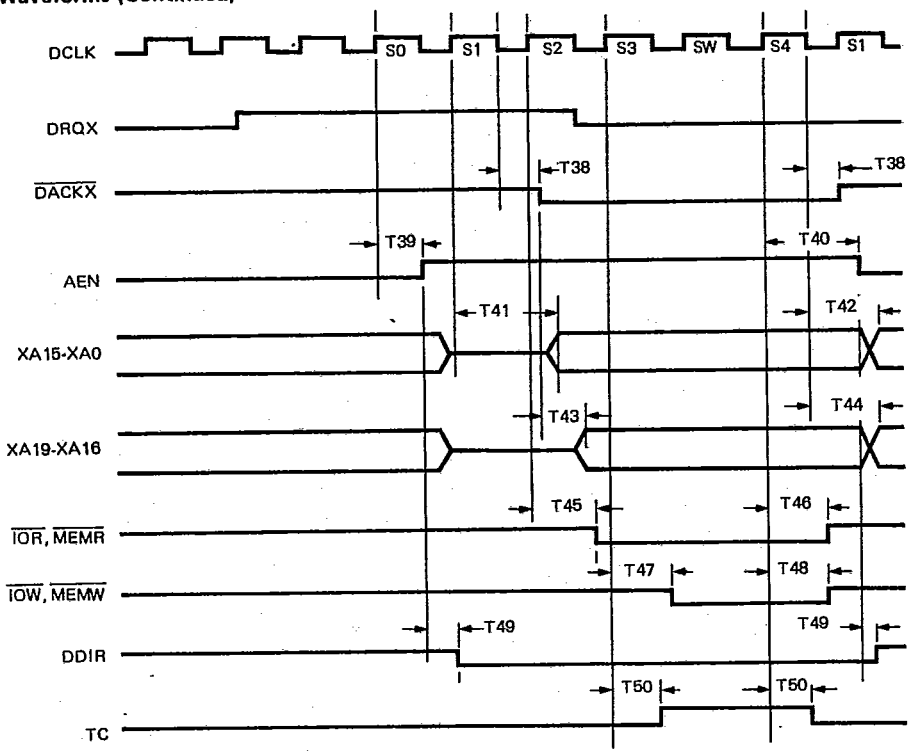
PC Mainboard

Timing Waveforms (Continued)



Read, Write Timing

Timing Waveforms (Continued)



DMA Cycle Timing